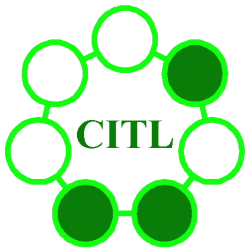


A Research on Improvement of Error Floor of ARA codes

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Motivation



■ ARA codes

- Linear time encoding
- Variable code length
- Rate compatible code
- Low threshold

■ High error floor of ARA codes

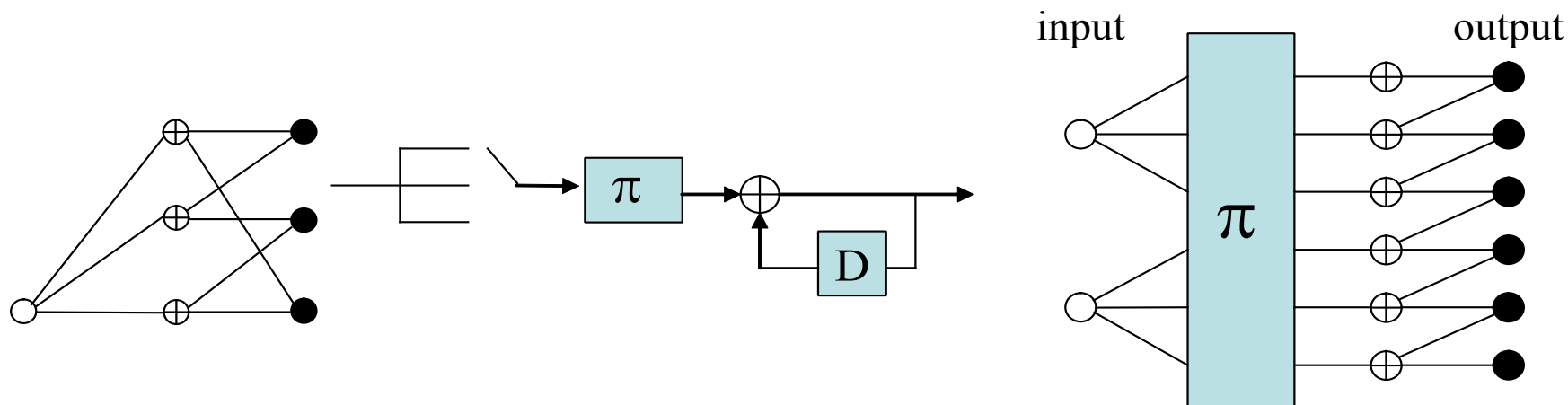
- Small minimum distance of ARA results in high error floor

■ Goal of the paper

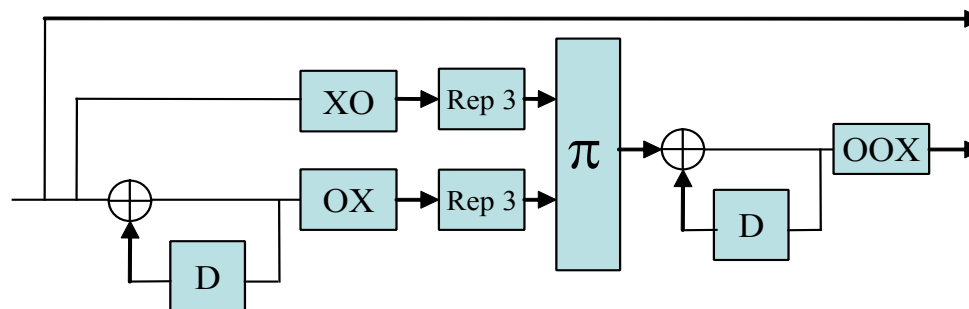
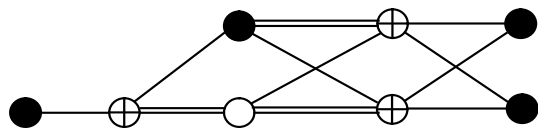
- Achieve improvement of error floor without loss of performance in waterfall and with a slight burden of complexity

■ RA codes

- Repetition + Accumulation
- Construction based on protograph
- Decoded using BP algorithm as a subclass of LDPC codes



■ Protograph and Encoder of ARA code



■ Parity check matrix

- Erasure bits due to intermediate bits and puncturing
- Reducing erasure bits for decoding convergence

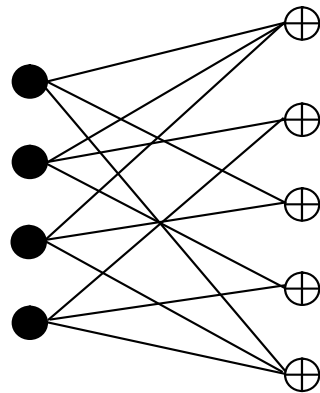
Information	Erasure	Parity
/	/	
	PEG Interleaver $(d_v, d_c) = (3, 3)$	/

■ Stopping set

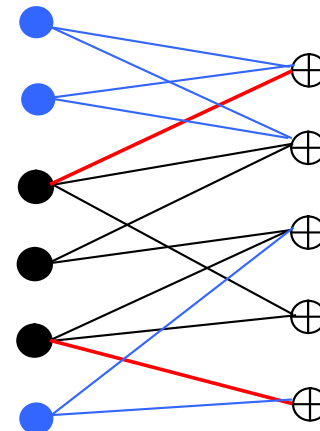
- A set of variable nodes whose neighbors are connected to the set at least twice
- No smaller size of stopping set than t ensures that minimum distance $d_{\min} \geq t$

■ EMD (Extrinsic message degree)

- Number of extrinsic check nodes
- A variable node set with large EMD requires additional nodes to be a stopping set

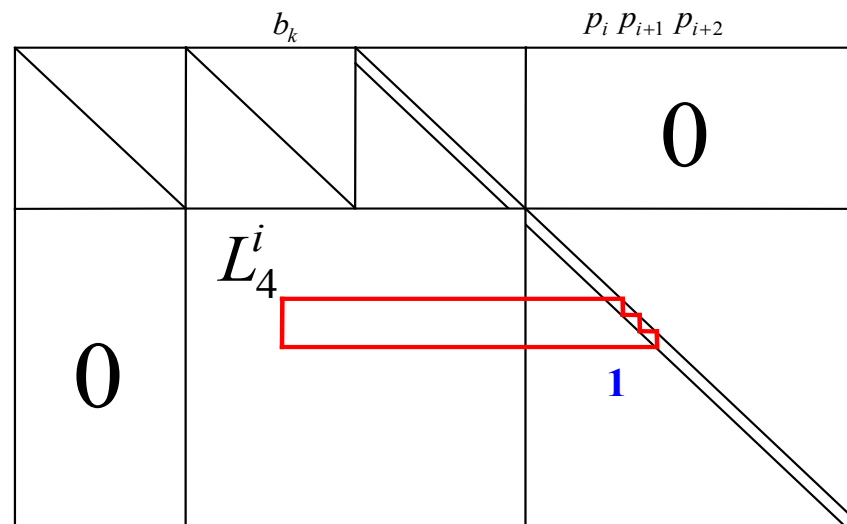
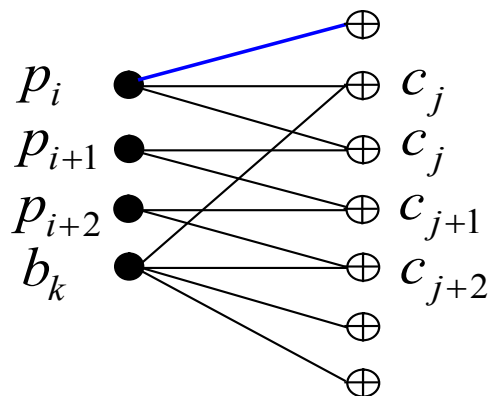


Stopping set of size 4



Stopping set with EMD=6

■ Consecutive parities cycle L_d



■ EMD of L_d

- $EMD(L_d) = Degree(b_k) - 2$
- Likely to be a small size of stopping set

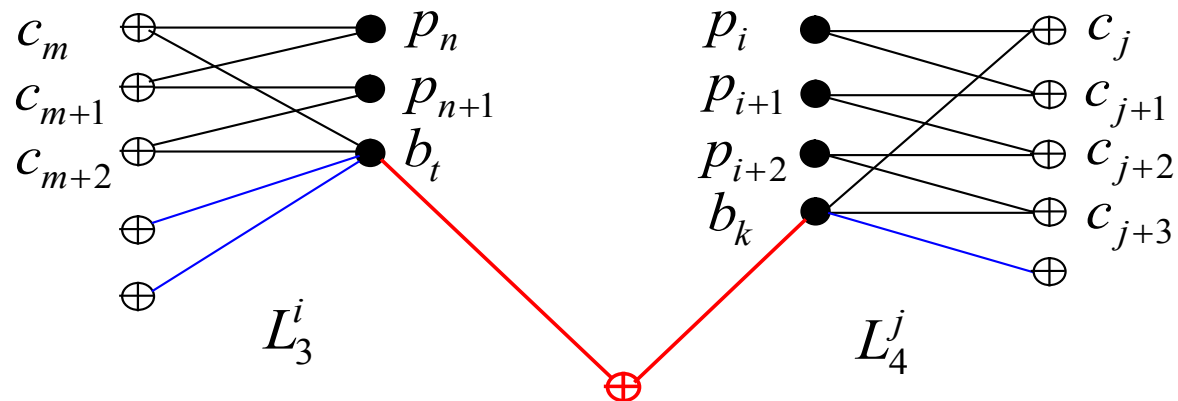
■ Union of L_d 's

- Some unions of L_d 's have interconnection
- Small size and small EMD for size
- Consider union of 2 consecutive cycle sets

■ EMD of union

- Deficient EMD of union

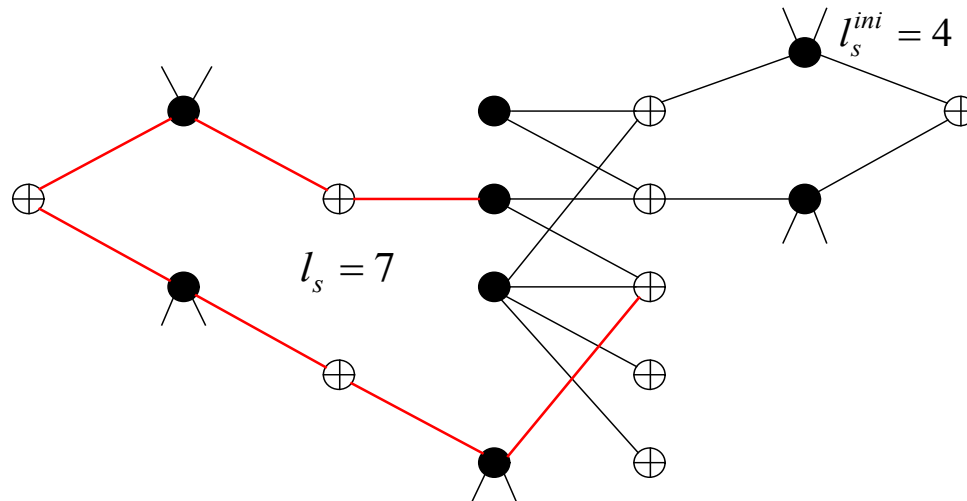
$$E_{Def}(i, j) = EMD(L_d^i) + EMD(L_d^j) - EMD(L_d^i \cup L_d^j)$$



Union of 2 consecutive cycle sets with size 7 and EMD 3

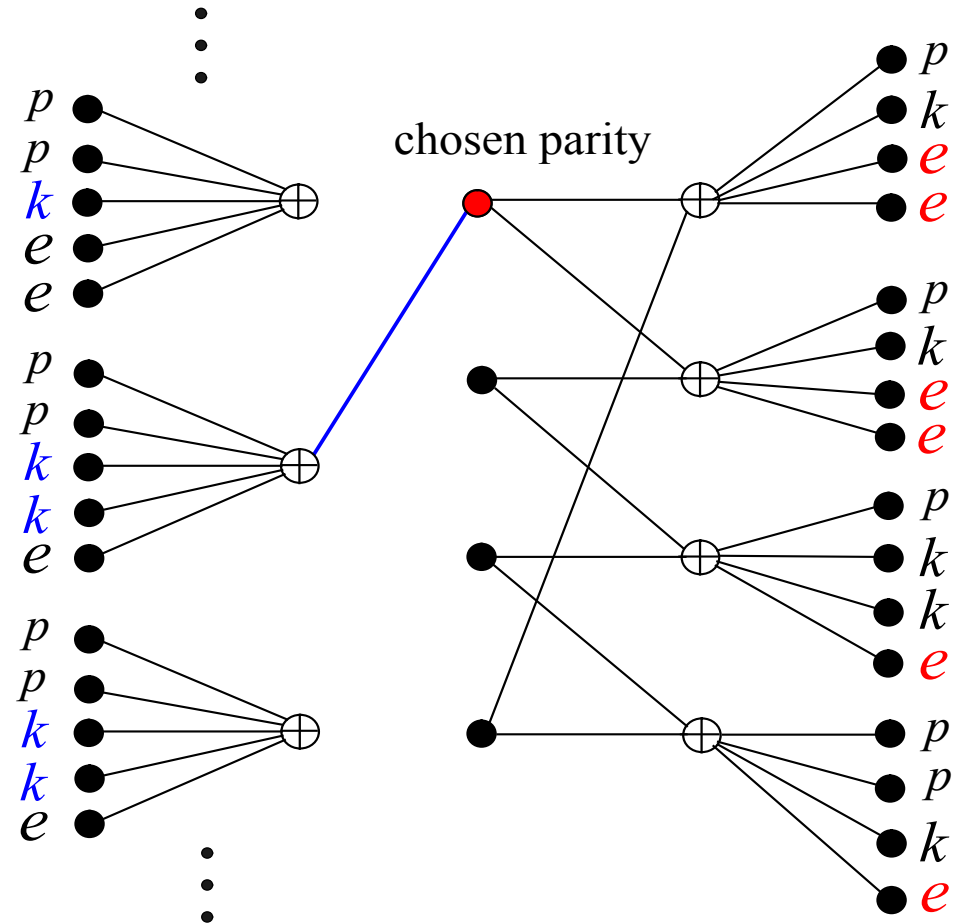
■ Self return distance l_s

- Smallest number of edges from L_d to L_d
- Large l_s will make more bit nodes involved when L_d and other bits node make up stopping set
- New edge does not decrease l_s

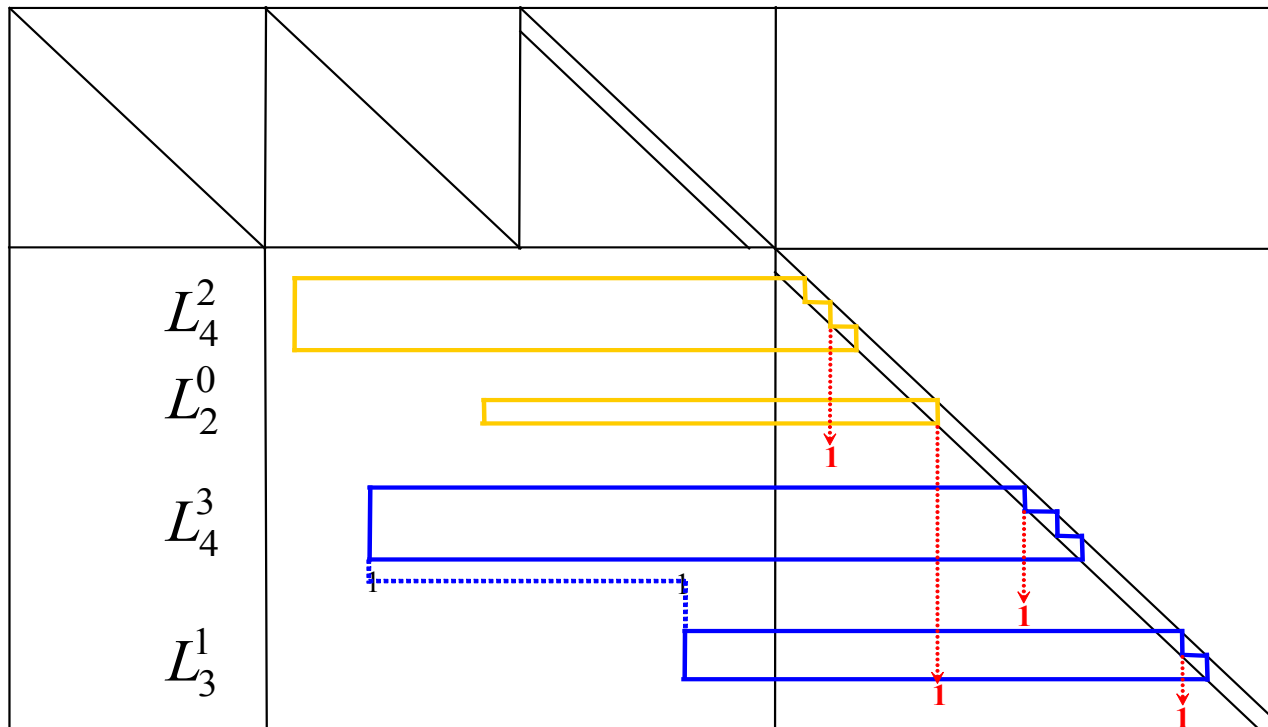


■ Criterion for new connection

- Selection of a parity bit
 - ✓ Erasure and information connectivity
- Selection of a check node
 - ✓ Erasure and information connectivity
 - ✓ Self return distance
 - ✓ EMD
 - ✓ Maximize resulting cycle length



- 1. Identify all the consecutive parity cycles, index from small size cycles
- 2. Evaluate initial $E_{Def}(i, j)$ and l_s^{ini}
- 3. Add new edge
 - For consecutive cycle sets with $E_{Def}(i, j) > 0$ until $E_{Def}(i, j) \leq 0$
 - Add new edge to an every loop except already added loop



$$E_{Def}(1,3) = 2$$

Add edge to L_3^1 and L_4^3

Add edge to other cycles

for L_2^0

for L_4^2



Simulation results(1)



■ Interleaver construction using PEG algorithm

- Local girth distribution (K=510, Rate=0.5)

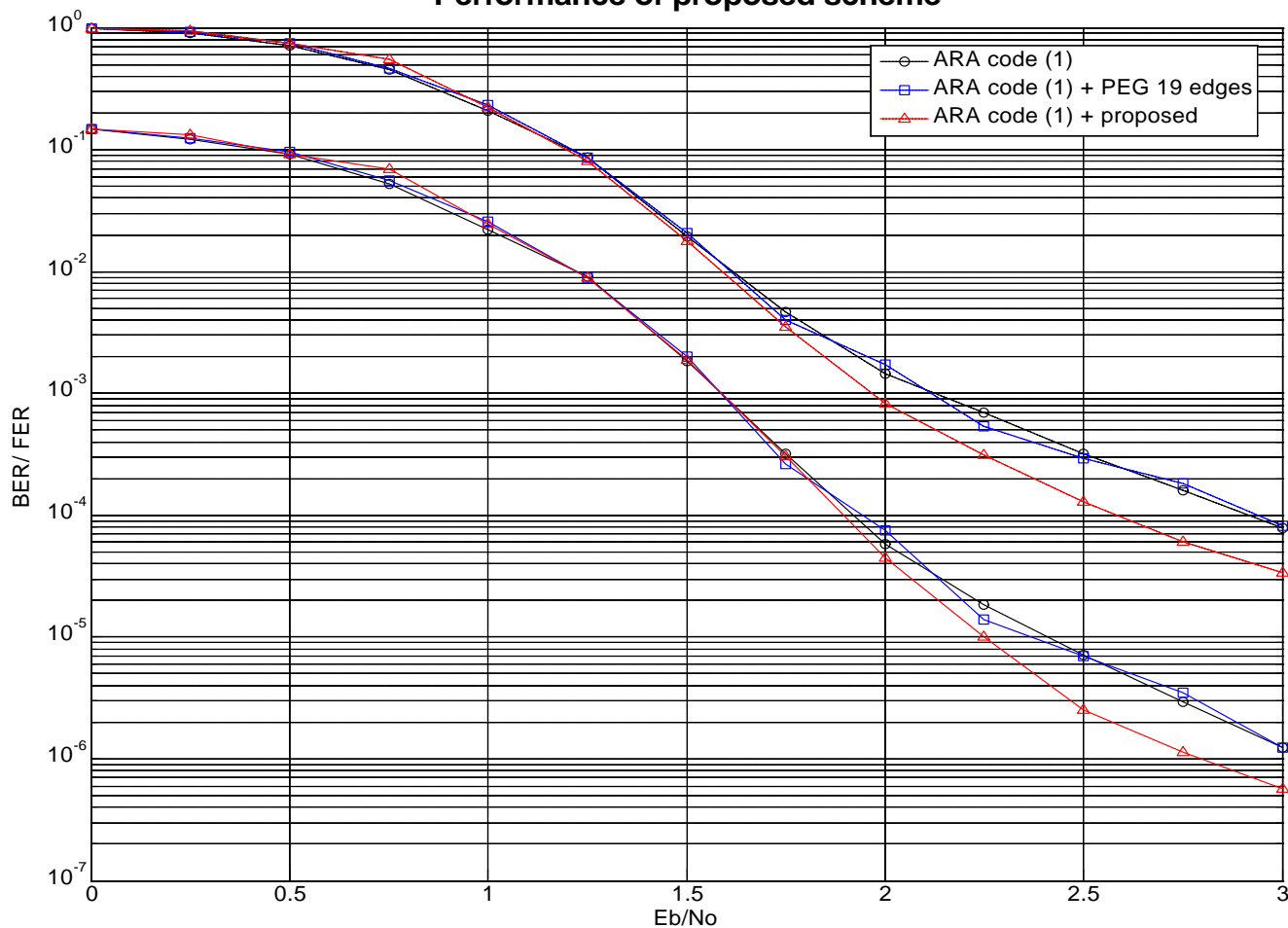
Local girth	4	6	8	10
ARA code (1)	23	247	602	147
ARA code (2)	8	111	456	444

- Consecutive parity cycle set distribution

	ARA code (1)	ARA code (2)
L_2	4	0
L_3	8	5
L_4	7	2
L_5	2	8

■ ARA code (1)

Performance of proposed scheme



	Number
L_2	4
L_3	8
L_4	7
L_5	2

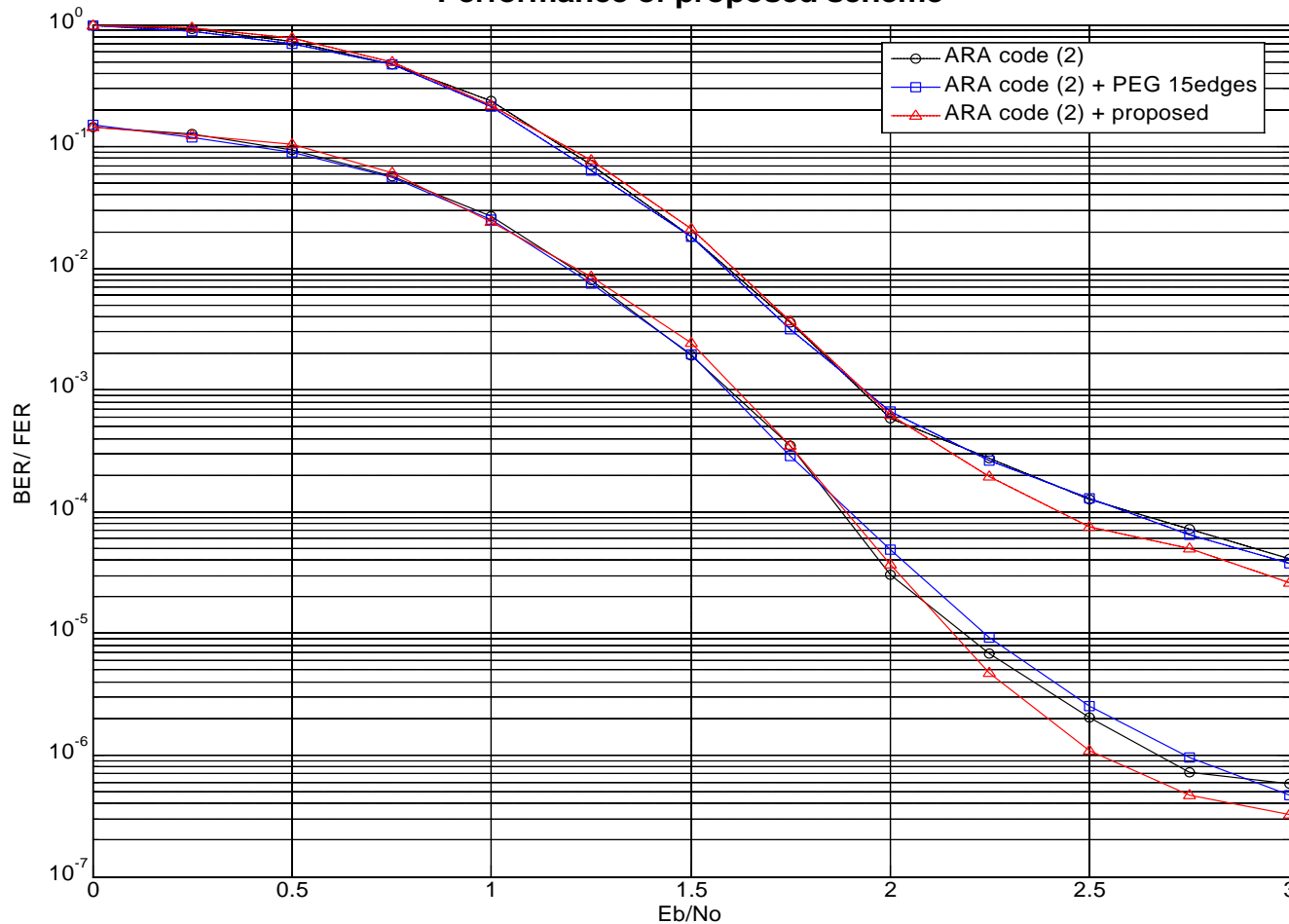
$K=510$, Rate=0.5

19 edges are added
and maximum 1 for
each cycle

At FER 10^{-4} , 0.35 dB
gain

ARA code (2)

Performance of proposed scheme



	Number
L_2	0
L_3	5
L_4	2
L_5	8

- K=510, Rate=0.5
- 15 edges are added and maximum 1 for each cycle
- At FER 10^{-4} , 0.15 dB gain



Conclusion



■ Improvement of Error floor

- Analysis of cycles with some part of the dual diagonal of ARA codes
- Supplement EMD's with the consecutive parities cycles

■ Some limits

- Need enough number of short consecutive parity cycles
- Cannot provide improvement when applying to a RA codes.

■ Further work

- Modification for RA codes and ARA codes with small number of short consecutive parity cycles.



Thank you