Performance Comparison of LDPC Convolutional Codes for Memory Size and Encoder Block Size



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LDPC Convolutional Codes



Parameters and Performance



Design of the Parity Check Matrix



Design of the Sub-Matrices

There are some methods... Idea from Quasi-Cyclic LDPC (**QC-LDPC**) block codes has been considered

Design a Good H(D)

$$H(D) = \begin{bmatrix} h_{1,1}(D) & \cdots & h_{1,c}(D) \\ \vdots & \ddots & \vdots \\ h_{c-b,1}(D) & \cdots & h_{c-b,c}(D) \end{bmatrix}$$
$$(c-b) \times c \text{ monomial matrix}$$

, where
$$h_{i,j}(D) = D^{q}, q = 0, \dots, M$$
.

From H(D) to H_i

$$H(D) = \begin{bmatrix} h_{1,1}(D) & \cdots & h_{1,c}(D) \\ \vdots & \ddots & \vdots \\ h_{c-b,1}(D) & \cdots & h_{c-b,c}(D) \end{bmatrix} \qquad H_2 \\ \vdots \\ H_M$$

Position of 1 in H_i = Position of D^i in H(D)All other positions in H_i : Put 0

From H(D) to H_i

Example



Matrix Expansion and Degree Distribution

Example: Comparing 3×6 **and** 6×12 **monomial matrix**



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Example: Comparing 3 × 6 and 6 × 12 monomial matrix



Sparse Monomial Matrix

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$$\boldsymbol{H}(D) = \begin{bmatrix} h_{1,1}(D) & \cdots & h_{1,c}(D) \\ \vdots & \ddots & \vdots \\ h_{c-b,1}(D) & \cdots & h_{c-b,c}(D) \end{bmatrix}$$

, where
$$h_{i,j}(D) = \begin{cases} D^q, & q = 0, \cdots, M \\ 0 \end{cases}$$

Contains a lot of zeros

To change (or increase) the encoder block size without changing the degree distribution of H'

Matrix Expansion Operation

Definition (Matrix expansion operation): Let $A = (a_{ij})$ be an $m \times n$ matrix and $B = (b_{ij})$ an $ml \times nl$ (0,1) matrix for some integer l > 1. We define an operation \circledast as

 $A \circledast B = C,$ where the ml × nl matrix $C = (c_{ij})$ is calculated as $c_{ij} = b_{ij} \cdot a_{\lfloor \frac{i-1}{l} + 1 \rfloor \lfloor \frac{j-1}{l} + 1 \rfloor}.$



Control Parameters for Simulation

Different number of delay blocks (memories) with fixed sub-matrix size Different sub-matrix size with fixed number of delay blocks

Similar Constraint Length with different sub-matrix size and delay block size

Simulation: Different Number of Delay Blocks



Simulation: Different Sub-Matrix Size



Simulation: Similar Constraint Length



Discussion

