



Construction of Irregular QC-LDPC Codes with Error-Floor Mitigation for Non-Terrestrial Links



Hyun Kim*, Gangsan Kim*, Hong-Yeop Song*, Hongjun Noh** and Chulho Lee **

* Yonsei University, Seoul, Republic of Korea

** LIG Defense & Aerospace, Seongnam-si, Republic of Korea

International Conference on ICT Convergence 2026

In this study, we propose an algebraic construction of irregular quasi-cyclic low-density parity-check (QC-LDPC) codes based on Golomb rulers. The construction guarantees a girth of at least 8 and avoids short cycles with low approximate cycle extrinsic message degree (ACE) values. We apply some CPM-level masking on the parity check matrix which diversifies the degree distribution. Simulation is used to confirm the error performance of the proposed codes before and after masking.

Introduction

- QC-LDPC codes [1] are widely adopted in communication standards due to their efficient implementation.
- In NTN [2], suppressing the error floor is important to reduce costly retransmissions.
- Avoiding short cycles and cycles with low ACE values helps improve error-floor performance [3,4].
- Greater degree-distribution diversity tends to improve waterfall performance, while increasing vulnerability to the error floor [5].

Construction of QC-LDPC Codes

- The $s \times t$ exponent matrix E_A is defined as

$$E_A = \begin{bmatrix} g_0 & 2g_0 & \cdots & tg_0 \\ g_1 & 2g_1 & \cdots & tg_1 \\ \vdots & \vdots & \ddots & \vdots \\ g_{s-1} & 2g_{s-1} & \cdots & tg_{s-1} \end{bmatrix}$$

where $g = \{g_0, g_1, g_2, \dots, g_{s-1}\}$ is an t -scaled Golomb ruler of length $L = g_{s-1} - g_0 = g_{s-1}$ satisfying the following two conditions:

i) Golomb ruler condition :

$$g_i - g_j \neq g_k - g_l, \quad i > j, k > l, \quad (i, j) \neq (k, l)$$

ii) t -scaled difference condition :

$$a(g_i - g_j) \neq b(g_k - g_l), \quad a, b \in \{1, 2, 3, \dots, t\}$$

Each exponent E_A is replaced by a $P \times P$ CPM with the corresponding cyclic shift, resulting in the $Ps \times Pt$ submatrix A .

- The $s \times s - 1$ exponent matrix E_B is constructed using a rectangular spiral pattern.

The following shows an example for $s = 6$:

$$E_B = \begin{bmatrix} \alpha & -1 & -1 & -1 & -1 \\ -1 & \alpha & -1 & -1 & \alpha \\ -1 & -1 & \alpha & \alpha & -1 \\ -1 & -1 & \alpha & -1 & -1 \\ -1 & \alpha & -1 & \alpha & -1 \\ \alpha & -1 & -1 & -1 & \alpha \end{bmatrix}$$

The non-null entries are set to $\alpha = 0$.

Each non-null entry is lifted to a $P \times P$ CPM, while each -1 entry is lifted to $P \times P$ zero matrix, resulting in the $Ps \times P(s - 1)$ submatrix B .

- The proposed $Ps \times P(t + s - 1)$ parity check matrix :

$$H = [A \mid B]$$

- CPM-Level Masking :

To diversify the variable-node degree distribution, selected non-zero entries in E_A are replaced by -1 .

Main Results

- **Theorem 1** : For $P > tL$, the proposed QC-LDPC code guarantees **girth ≥ 8**
- **Theorem 2** : For $P > tL$, every cycle in the Tanner graph of the proposed code satisfies **$\eta \geq 2(s - 2)$**

Therefore, the proposed construction prevents short cycles and excludes cycles with low ACE values.

- **Simulation parameters :**

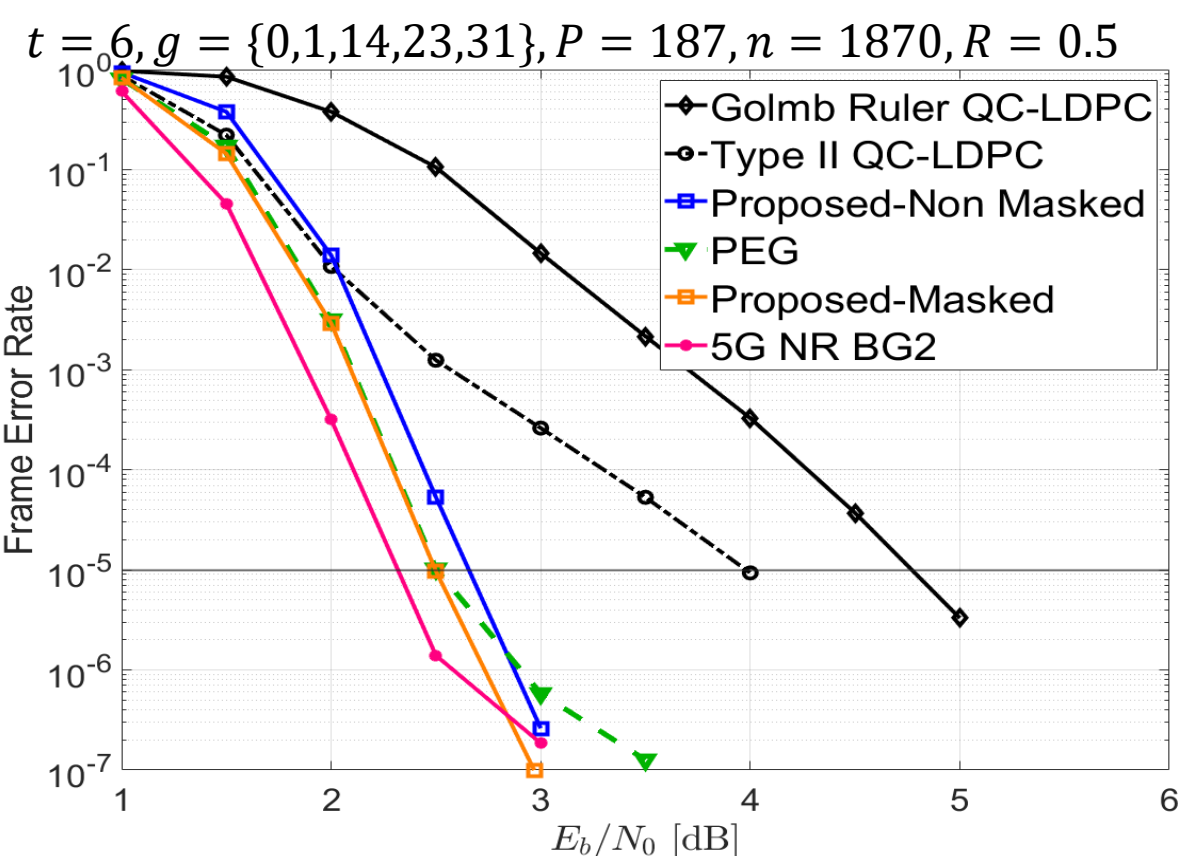


Fig 1. FER performance of rate 1/2 and length around 1,800

Code Construction	Girth g	Min. ACE (η_{min}) by Cycle Length		
		8-cycle	10-cycle	12-cycle
Golomb Ruler QC-LDPC	8	4	5	6
Type-II QC-LDPC	8	6	4	4
PEG-based	8	3	3	3
Proposed 5-mark	8	9	6	9
Proposed-Masked 5-mark	8	7	5	5
5G NR BG2	8	17	19	22

Table I. MINIMUM ACE (η) BY CYCLE LENGTH FOR FIG. 1

Conclusion

The proposed codes achieve competitive waterfall and error-floor performance compared with other LDPC codes.

REFERENCES

- [1] M. P. C. Fossorier, "Quasicyclic low-density parity-check codes from circulant permutation matrices," IEEE Trans. Inf. Theory, vol. 50, no. 8, pp. 1788–1793, Aug. 2004..
- [2] 3GPP, "Solutions for NR to support non-terrestrial networks (NTN)," 3GPP TR 38.821, V16.0.0, Dec. 2019.
- [3] T. Richardson, "Error floors of LDPC codes," in Proc. 41st Annu. Allerton Conf. Commun., Control, Comput., 2003, pp. 1426–1435.
- [4] T. Tian, C. R. Jones, J. D. Villasenor, and R. D. Wesel, "Selective avoidance of cycles in irregular LDPC code construction," IEEE Transactions on Communications, vol. 52, no. 8, pp. 1242–1247, Aug. 2004.
- [5] T. J. Richardson, M. A. Shokrollahi, and R. L. Urbanke, "Design of capacity-approaching irregular low-density parity-check codes," IEEE Trans. Inf. Theory, vol. 47, no. 2, pp. 619–637, Feb. 2001.